SONY

Diagonal 5.867 mm (Type 1/3.06) 13Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX214-0AQH5-C

General description and application

IMX214 is a diagonal 5.867mm (Type 1/3.06) 13 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor-RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is emproyed. By introducing spacially varying exposure technology, high dynamic range still pictures and movies are achievable. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.7 V, digital 1.0 V and 1.8 V for input/output interface and achieves low power consumption.
IMX214 is designed for use in cellular phones or tablet devices*[1].

Functions and Features

- ◆Back-illuminated and stacked CMOS image sensor “Exmor-RS™”
- ◆Single Frame High Dynamic Range (HDR) with equivalent full pixels.
- ◆High signal to noise ratio (SNR).
- ◆Full resolution @30fps (Nornmal / HDR). 4K2K @30fps (Normal / HDR) 1080p @60fps (Normal / HDR)
- ◆Output video format of RAW10/8, COMP8/6.
- ◆Pixel binning readout and H/V sub-sampling function.
- ◆Advanced Noise Reduction (Chroma noise reduction and luminance noise reduction).
- ◆Independent flipping and mirroring.
- ◆CSI-2 serial data output (MIPI 2lane/4lane, Max. 1.2Gbps/lane, D-PHY spec. ver. 1.1 compliant)
- ◆2-wire serial communication.
- ◆Two PLLs for independent clock generation for pixel control and data output interface.
- ◆Advanced Noise Reduction.
- ◆Dynamic Defect Pixel Correction.
- ◆Zero shutter lag.
- ◆Power-on reset function
- ◆Dual sensor synchronization operation.
- ◆8K bit of OTP ROM for users.
- ◆Built-in temperature sensor

NOTE)
1. When using this product for another application, Sony does not guarantee the quality and reliability of product. Therefore, don’t use this for applications other than cellular phone and Tablet PCs. Consult your Sony sales representative if you have any questions.

Exmor RS™

* "Exmor RS" is a trademark of Sony Corporation. The "Exmor RS" is a Sony’s CMOS image sensor with high-resolution, high-performance and compact size by replacing a supporting substrate in "Exmor R" which changed fundamental structure of “Exmor” pixel adopted column parallel A/D converter to back-illuminated type, with layered chips formed signal processing circuits.

Sony reserves the right to change products and specifications without prior notice.
This information does not convey any license by any implication or otherwise under any patents or other right.
Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

CONFIDENTIAL

Device Structure

◆CMOS image sensor
◆Image size : Diagonal 5.867 mm (Type 1/3.06)
◆Total number of pixels : 4224 (H) × 3200 (V) approx. 13.51 M pixels
◆Number of effective pixels : 4224 (H) × 3136 (V) approx. 13.25 M pixels
◆Number of active pixels : 4208 (H) × 3120 (V) approx. 13.13 M pixels
◆Chip size : 6.100 mm (H) × 4.524 mm (V)
◆Unit cell size : 1.12 µm (H) × 1.12 µm (V)
◆Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	refer to Vss level
Supply voltage (digital)	VDIG	-0.3 to +1.8	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to +3.3	V	
Output voltage (digital)	VO	-0.3 to +3.3	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

CONFIDENTIAL

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.7 + 0.2/-0.1 V	V	refer to Vss level
Supply voltage (digital)	VDIG	1.0 +0.15/-0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

Excellence Commsen

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

CONFIDENTIAL

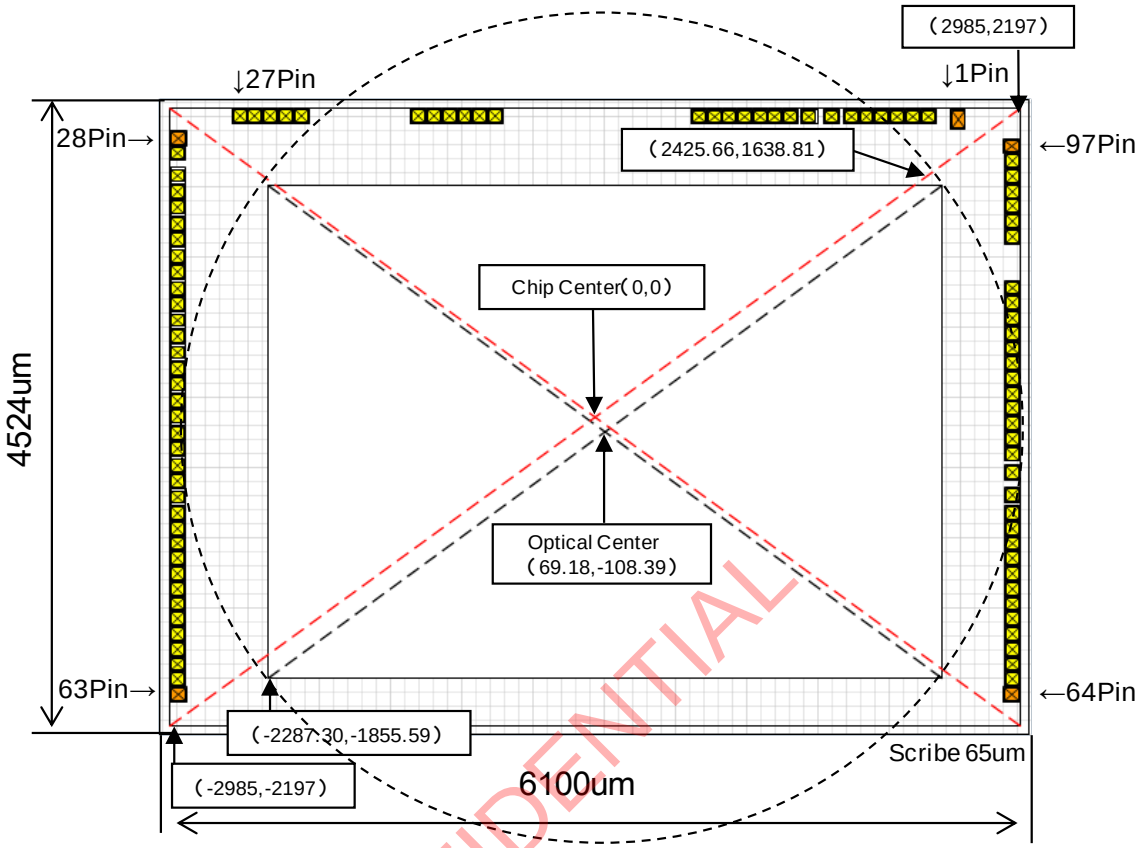
Contents

CONFIDENTIAL

CONFIDENTIAL

CONFIDENTIAL

Chip Center and Optical Center



※1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account
※2 Some PADs are located in image circle.

Figure 1 Chip Center and Optical Center (x and y coordinates in µm)

CONFIDENTIAL

Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VDDSUB	2548.50	2122.00
2	VSSHSN1	2332.48	2140.25
3	VDDHSN1	2224.96	2140.25
4	VSSLSC1	2117.44	2140.25
5	VDDLSC1	2009.92	2140.25
6	TESTOUT	1902.40	2140.25
7	GPO	1794.88	2140.25
8	SDAM	1660.84	2140.25
9	SCLM	1503.32	2140.25
10	VDDMIO1	1369.28	2140.25
11	VSSLSC2	1261.76	2140.25
12	VDDLSC2	1154.24	2140.25
13	POREN	1046.72	2140.25
14	SWDIO	939.20	2140.25
15	SWTCK	831.68	2140.25
16	TENABLE	724.16	2140.25
17	TEST1	-717.40	2140.25
18	TEST2	-824.92	2140.25
19	TEST3	-932.44	2140.25
20	VDDLSC3	-1039.96	2140.25
21	VSSLSC3	-1147.48	2140.25
22	VDDMIO2	-1255.00	2140.25
23	VDDHPL	-2062.52	2140.25
24	VSSHPL	-2170.04	2140.25
25	VPI1	-2277.56	2140.25
26	VRL1	-2385.08	2140.25
27	VSSHSN2	-2492.60	2140.25
28	VDDLSC4	-2922.25	1989.82
29	VSSLSC4	-2928.25	1882.30
30	VSSLIO1	-2928.25	1774.78
31	DMO3P	-2928.25	1659.58
32	DMO3N	-2928.25	1544.38
33	DMO1P	-2928.25	1429.18
34	DMO1N	-2928.25	1313.98
35	VSSLIO2	-2928.25	1198.78
36	VDDLIO1	-2928.25	1083.58
37	VDDLSC5	-2928.25	968.38
38	VSSLSC5	-2928.25	853.18
39	DCKP	-2928.25	737.98
40	DCKN	-2928.25	622.78
41	VSSLSC6	-2928.25	507.58
42	VDDLSC6	-2928.25	392.38
43	VDDLIO2	-2928.25	277.18
44	VSSLIO3	-2928.25	161.98
45	DMO2P	-2928.25	46.78
46	DMO2N	-2928.25	-68.42
47	DMO4P	-2928.25	-183.62
48	DMO4N	-2928.25	-298.82
49	VSSLIO4	-2928.25	-414.02
50	VDDMMD1	-2928.25	-579.22

No.	Symbol	X	Y
51	VSSLSC7	-2928.25	-686.74
52	VSSLSC8	-2928.25	-794.26
53	VDDLSC7	-2928.25	-901.78
54	VDDLSC8	-2928.25	-1009.30
55	VSSLSC9	-2928.25	-1116.82
56	VSSLSC10	-2928.25	-1224.34
57	VDDLSC9	-2928.25	-1331.86
58	VSSLCN1	-2928.25	-1439.38
59	VDDLCN1	-2928.25	-1546.90
60	VSSLCB1	-2928.25	-1654.42
61	VDDHCM1	-2928.25	-1761.94
62	VSSHSN3	-2928.25	-1869.46
63	VDDHSN2	-2922.25	-1976.98
64	VDDHSN3	2922.25	-1976.98
65	VSSHSN4	2928.25	-1869.46
66	VDDHCM2	2928.25	-1761.94
67	VSSLCB2	2928.25	-1654.42
68	VDDLCN2	2928.25	-1546.90
69	VSSLCN2	2928.25	-1439.38
70	VDDLSC10	2928.25	-1331.86
71	VSSLSC11	2928.25	-1224.34
72	FSTROBE	2928.25	-1116.82
73	SLASEL	2928.25	-1009.30
74	VSSLSC12	2928.25	-901.78
75	VDDLSC11	2928.25	-794.26
76	VDDMIO3	2928.25	-686.74
77	SDA	2928.25	-552.70
78	SCL	2928.25	-395.18
79	VDDHAN	2928.25	-261.14
80	VSSHAN	2928.25	-153.62
81	TVMON	2928.25	-46.10
82	TVCDSIN	2928.25	61.42
83	VRL2	2928.25	168.94
84	VPI2	2928.25	276.46
85	VSSHCP	2928.25	383.98
86	VDDHCP	2928.25	491.50
87	VDDLSC12	2928.25	599.02
88	VSSLSC13	2928.25	706.54
89	VREN	2928.25	817.06
90	VDDHVR	2928.25	924.58
91	VDDMIO4	2928.25	1288.94
92	VSSLSC14	2928.25	1396.46
93	VDDLSC13	2928.25	1503.98
94	REGEN	2928.25	1611.50
95	INCK	2928.25	1719.02
96	XPORCD	2928.25	1826.54
97	XCLR	2922.25	1934.06

CONFIDENTIAL

Pin Description

Table 2 Pin Description

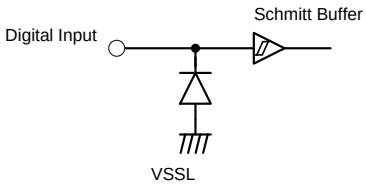
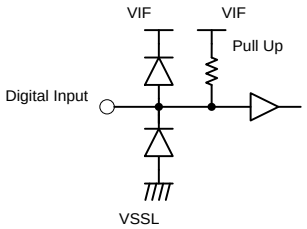
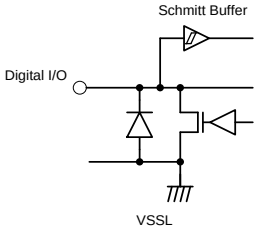
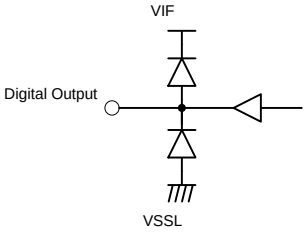
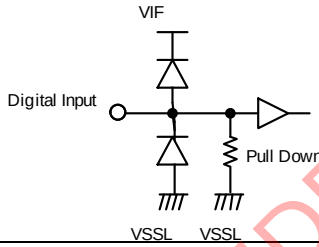
No.	Symbol	I/O	A/D	Description	Remarks
1	VDDSUB	Power	D	VANA power supply	
2	VSSHSN1	GND	A	VANA GND	
3	VDDHSN1	Power	A	VANA power supply	
4	VSSLSC1	GND	D	VDIG GND	
5	VDDLSC1	Power	D	VDIG power supply	
6	TESTOUT	O	D	Digital output	NC
7	GPO	O	D	Digital output	NC
8	SDAM	I/O	D	Digital I/O	NC
9	SCLM	I/O	D	Digital I/O	NC
10	VDDMIO1	Power	D	VIF power supply	
11	VSSLSC2	GND	D	VDIG GND	
12	VDDLSC2	Power	D	VDIG power supply	
13	POREN	I	D	Digital input	NC (pull-up)
14	SWDIO	I/O	D	Digital I/O	NC (pull-up)
15	SWTCK	I	D	Digital input	NC (pull-down)
16	TENABLE	I	D	Digital input	NC (pull-down)
17	TEST1	I	D	Digital input	NC (pull-down)
18	TEST2	I	D	Digital input	NC (pull-down)
19	TEST3	I	D	Digital input	NC (pull-down)
20	VDDLSC3	Power	D	VDIG power supply	
21	VSSLSC3	GND	D	VDIG GND	
22	VDDMIO2	Power	D	VIF power supply	
23	VDDHPL	Power	A	VANA power supply	
24	VSSHPL	GND	A	VANA GND	
25	VPI1	Power	A	Analog input	See Reference sircuit schematics Figure3 or Pigure4
26	VRL1	Minus	A	Analog input	Connect VRL2
27	VSSHSN2	GND	A	VANA GND	
28	VDDLSC4	Power	D	VDIG power supply	
29	VSSLSC4	GND	D	VDIG GND	
30	VSSLIO1	GND	D	VDIG GND	
31	DMO3P	O	D	Digital output	MIPI output (DATA+)
32	DMO3N	O	D	Digital output	MIPI output (DATA–)
33	DMO1P	O	D	Digital output	MIPI output (DATA+)
34	DMO1N	O	D	Digital output	MIPI output (DATA–)
35	VSSLIO2	GND	D	VDIG GND	
36	VDDLIO1	Power	D	VDIG power supply	
37	VDDLSC5	Power	D	VDIG power supply	
38	VSSLSC5	GND	D	VDIG GND	
39	DCKP	O	D	Digital output	MIPI output (CLK+)
40	DCKN	O	D	Digital output	MIPI output (CLK-)
41	VSSLSC6	GND	D	VDIG GND	
42	VDDLSC6	Power	D	VDIG power supply	
43	VDDLIO2	Power	D	VDIG power supply	
44	VSSLIO3	GND	D	VDIG GND	
45	DMO2P	O	D	Digital output	MIPI output (DATA+)
46	DMO2N	O	D	Digital output	MIPI output (DATA–)
47	DMO4P	O	D	Digital output	MIPI output (DATA+)
48	DMO4N	O	D	Digital output	MIPI output (DATA–)

CONFIDENTIAL

No.	Symbol	I/O	A/D	Description	Remarks
49	VSSLIO4	GND	D	VDIG GND	
50	VDDMMD1	Power	D	VIF power supply	
51	VSSLSC7	GND	D	VDIG GND	
52	VSSLSC8	GND	D	VDIG GND	
53	VDDLSC7	Power	D	VDIG power supply	
54	VDDLSC8	Power	D	VDIG power supply	
55	VSSLSC9	GND	D	VDIG GND	
56	VSSLSC10	GND	D	VDIG GND	
57	VDDLSC9	Power	D	VDIG power supply	
58	VSSLCN1	GND	D	VDIG GND	
59	VDDLCN1	Power	D	VDIG power supply	
60	VSSLCB1	GND	D	VDIG GND	
61	VDDHCM1	Power	A	VANA power supply	
62	VSSHSN3	GND	A	VANA GND	
63	VDDHSN2	Power	A	VANA power supply	
64	VDDHSN3	Power	A	VANA power supply	
65	VSSHSN4	GND	A	VANA GND	
66	VDDHCM2	Power	A	VANA power supply	
67	VSSLCB2	GND	D	VDIG GND	
68	VDDLCN2	Power	D	VDIG power supply	
69	VSSLCN2	GND	D	VDIG GND	
70	VDDLSC10	Power	D	VDIG power supply	
71	VSSLSC11	GND	D	VDIG GND	
72	FSTROBE	O	D	Digital output	Flash strobe
73	SLASEL	I	D	Digital input	I2C slave address select
74	VSSLSC12	GND	D	VDIG GND	
75	VDDLSC11	Power	D	VDIG power supply	
76	VDDMIO3	Power	D	VIF power supply	
77	SDA	I/O	D	Digital I/O	I2C pin
78	SCL	I/O	D	Digital I/O	I2C pin
79	VDDHAN	Power	A	VANA power supply	
80	VSSHAN	GND	A	VANA GND	
81	TVMON	O	A	Analog output	NC
82	TVCDSIN	I	A	Analog input	NC
83	VRL2	Minus	A	Analog input	Connect VRL1
84	VPI2	Power	A	Analog input	See Reference sircuit schematics Figure3 or Pigure4
85	VSSHCP	GND	A	VANA GND	
86	VDDHCP	Power	A	VANA power supply	
87	VDDLSC12	Power	D	VDIG power supply	
88	VSSLSC13	GND	D	VDIG GND	
89	VREN	I	D	VDIG GND	
90	VDDHVR	Power	A	VIF power supply	
91	VDDMIO4	Power	D	VIF power supply	
92	VSSLSC14	GND	D	VDIG GND	
93	VDDLSC13	Power	D	VDIG power supply	
94	REGEN	O	D	Digital input	Regulator enable control
95	INCK	I	D	Digital input	Clock input
96	XPORCD	I	D	Digital input	NC (pull-down)
97	XCLR	I	D	Digital input	Chip clear (pull-up)

CONFIDENTIAL

Input/Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK (EXTCLK)		XCLR	
SCL SDA		REGEN FSTROBE	
SLASEL			

VDDH : 2.7 V power supply
VSSH : 2.7 V GND

VIF : 1.8 V power supply
VSSL : VDIG GND

Figure 2 Input/Output Equivalent Circuit

CONFIDENTIAL

Peripheral Circuit Diagram

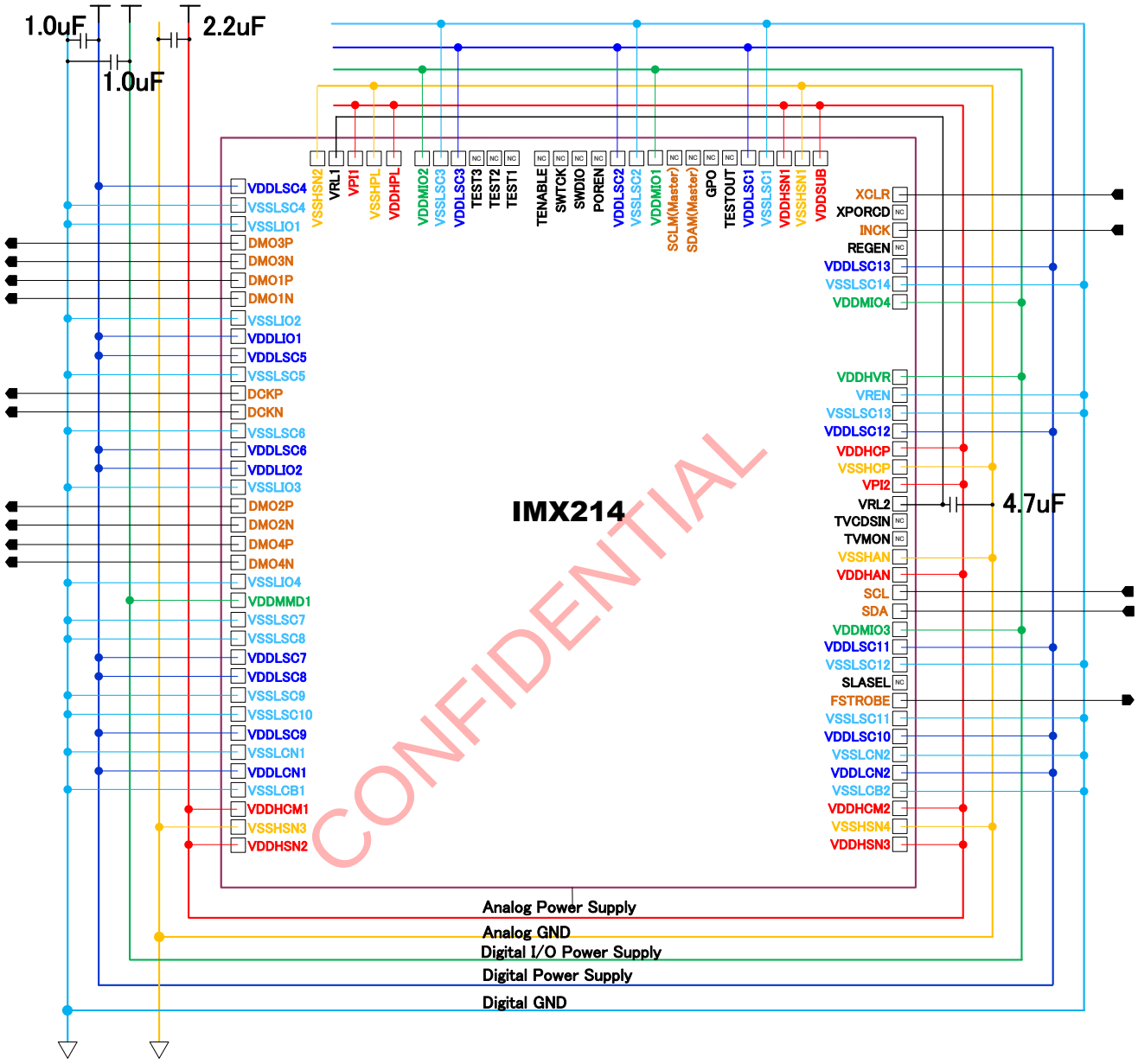


Figure 3 Reference circuit schematics(Default recommendation)
VPI1,2(pixel power supplies) are externally supplied.

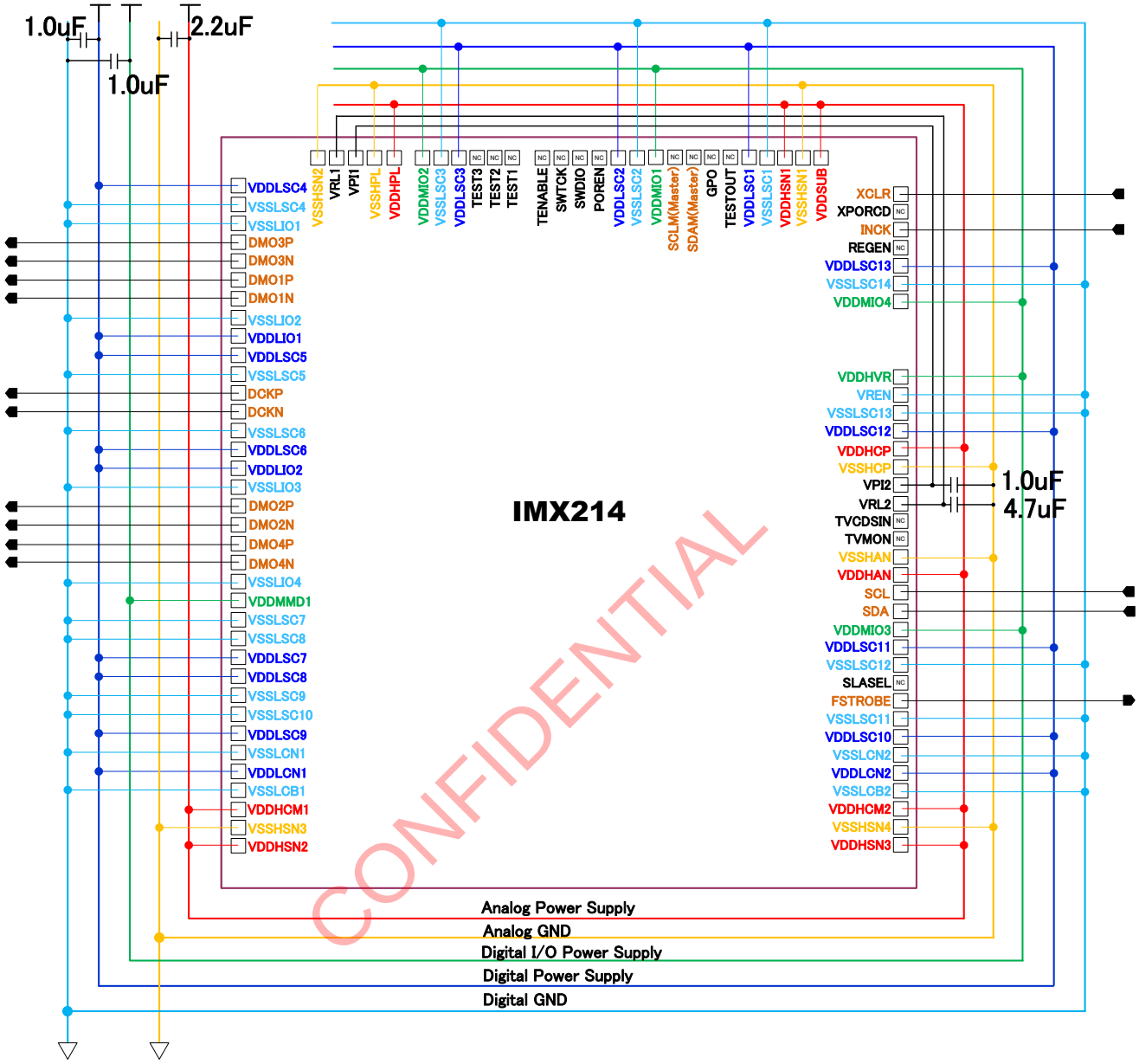


Figure 4 Reference circuit schematics
VPI1,2 (pixel power supplies) are Internally supplied

Functional Description

System Outline

IMX214 is a CMOS active pixel type image sensor which adopts the Exmor RS™ technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A one time programmable memory is embedded in the chip for storing the user data.It has 8 K-bit for users, 10 K-bit as a whole.

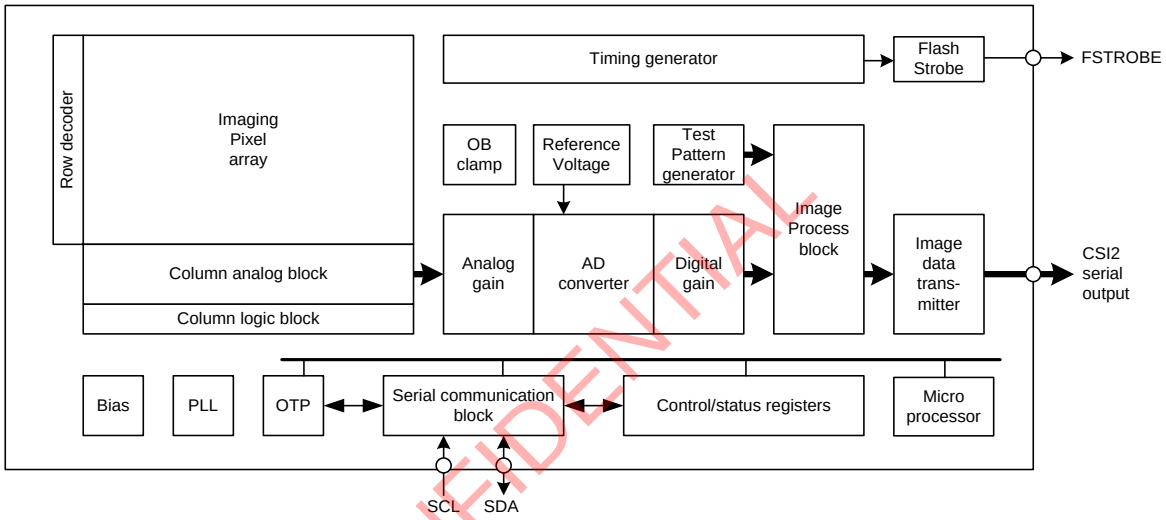


Figure 5 Overview of functional block diagram

CONFIDENTIAL

Control register setting by the serial communication

The IMX can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

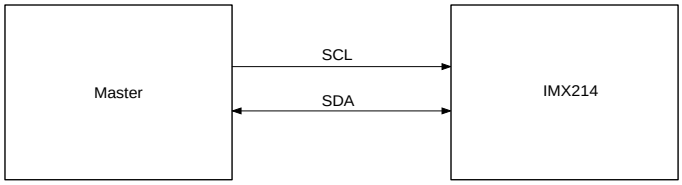


Figure 6 2-wire serial communication

2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I2C fast-mode compatible interface, and the data transfer protocol is I2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX.

CONFIDENTIAL

Table 3 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX214 are mapped on the 16-bit address space and following SMIA standard for the register categories shown as below. Detail regisrter information is shown in RegisterMap

Table 4 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Parameter limit register Read Only static resister
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

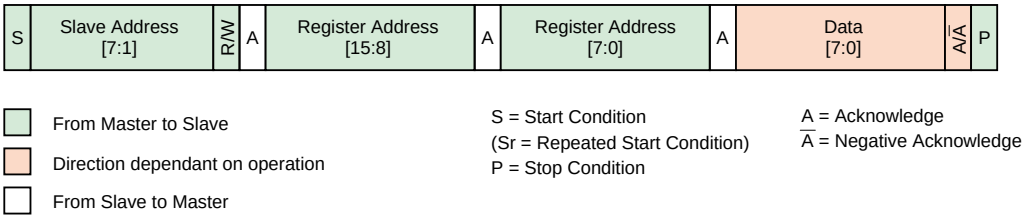
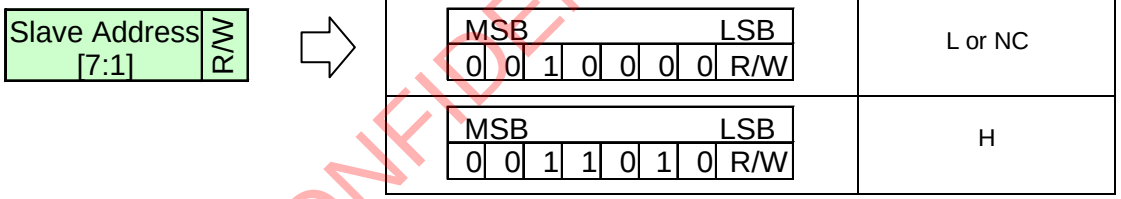


Figure 7 2-wire serial communication protocol

IMX214 has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.



R/W shows the direction of communication.the

Figure 8 Slave address

CONFIDENTIAL

Table 5 R/W bit

R/W bit	direction of communication
0	Write (Master→Sensor)
1	Read (Sensor →Master)

Clock generation and PLL

IMX214 equips embedded PLL to generate the necessary internal clocks and CSI2 tranmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

Clock System Diagram

The PLL circuit of IMX214 can generate a clock signal at a frequency ranging from 338 MHz up to 1200 MHz based on an input clock of 6 MHz to 27 MHz.
PLL block contains pre divider circuit with ratio 1/1 to 1/15 at the input side of the PLL, and a multiplier of 12 to 1200 times which can be set as long as the PLL oscillator frequency is kept within the specified range.

IMX214 is designed to operate with single PLL mode or dual PLL mode. In most cases of application, the single mode is recommended and can satisfy required mode specification. However, in such a case that internal operation constraints cause excessive bit rate under a given ISP specification and / or fine tuning of MIPI bit rate for EMC frequency are required, the dual mode operation can be an option to consider.

.

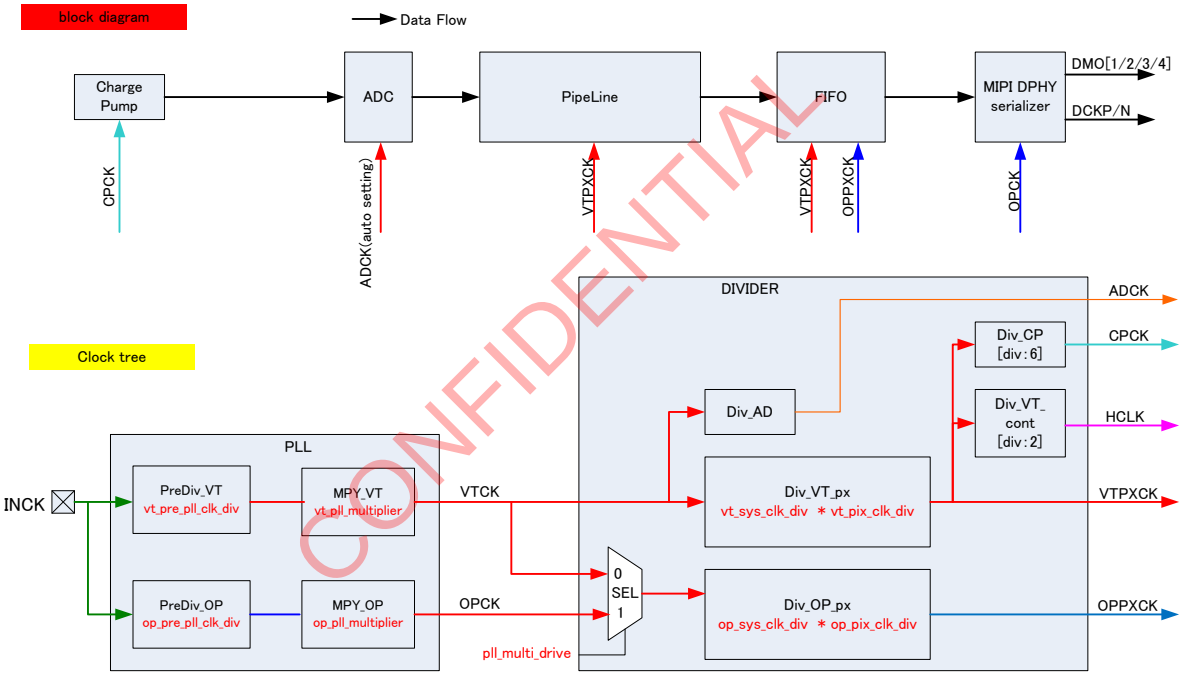


Figure 9 Clock System Diagram (PLL single mode)

CONFIDENTIAL

Description of operation clocks

The followings are general discriptions for each clock.See Application Note for more detail.

INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

VTCK, OPCK : PLL output

These clocks are the root of all the operation clocks in IMX214 and it designates the data rate.
DCKP/DCKN; CSI2 interface clock is generated from OPCK by dividing into 1/2 (or1/4) frequency since the interface is operated in double data rate format.

VTPXCK Clock

The clock for internal image processing is generated by dividing into 1/10, 1/12, 1/14, 1/16, 1/18, 1/20, 1/24, 1/28, 1/36 or 1/40 frequency. This clock is used as the base of integration time, frame rate, and etc.

OPPXCK Clock

The clock for internal image processing is generated by dividing into 1/6, 1/8, 1/10, 1/12, 1/14, 1/16, 1/20, 1/24 or 1/28 frequency according to the word length of the CSI2 interface. This clock is designating the pixel rate and etc.

CONFIDENTIAL

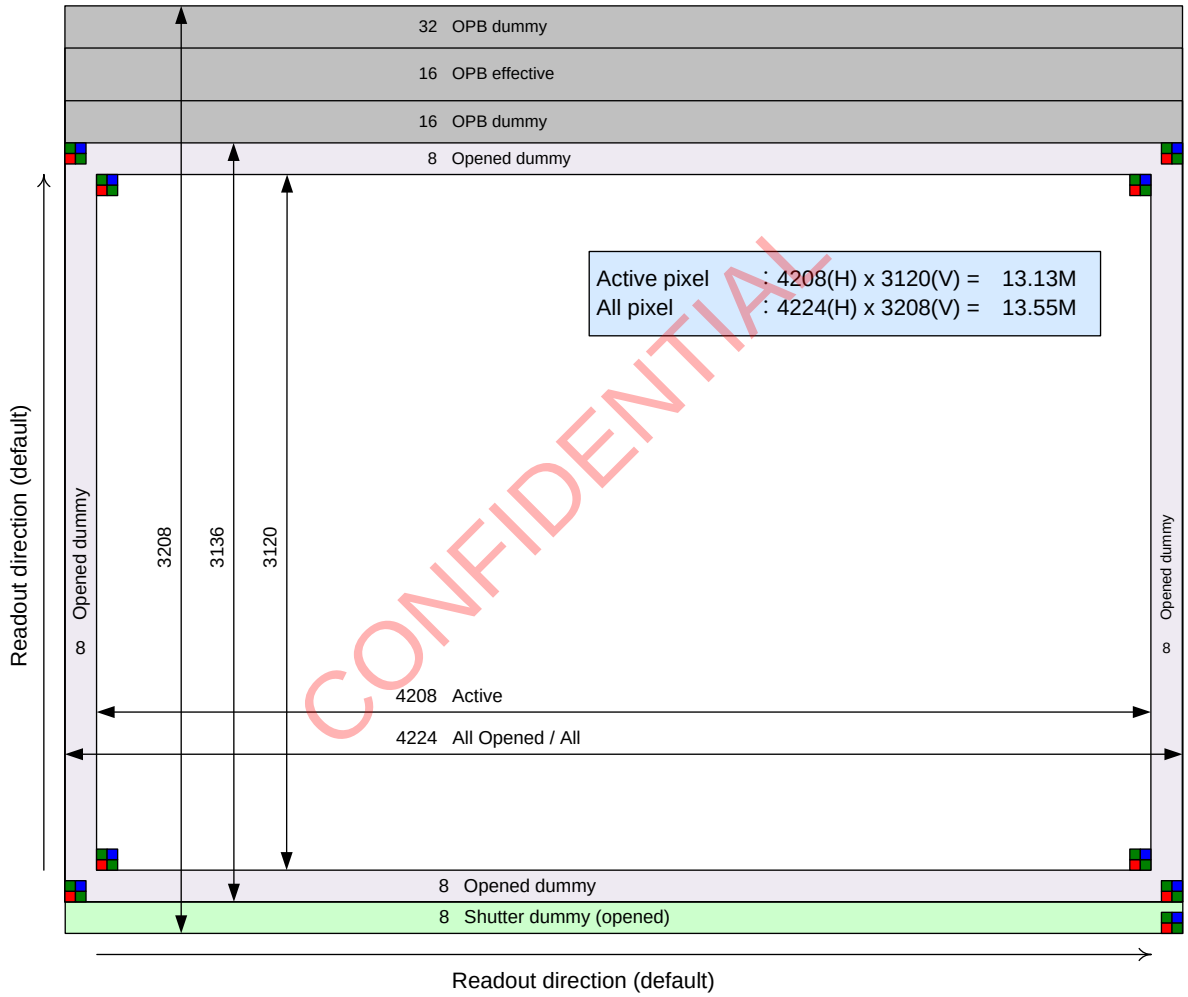
Image Readout Operation

By settimg the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX214 outputs the image data.

See Application Notes for more details of each function.

Phyical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.



CONFIDENTIAL

Figure 10 physical alignment of the imaging pixel array

Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively.

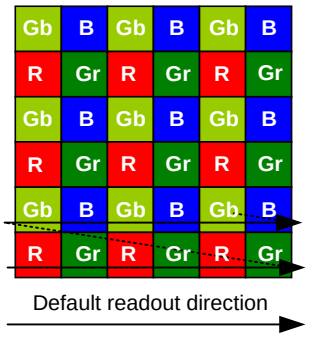
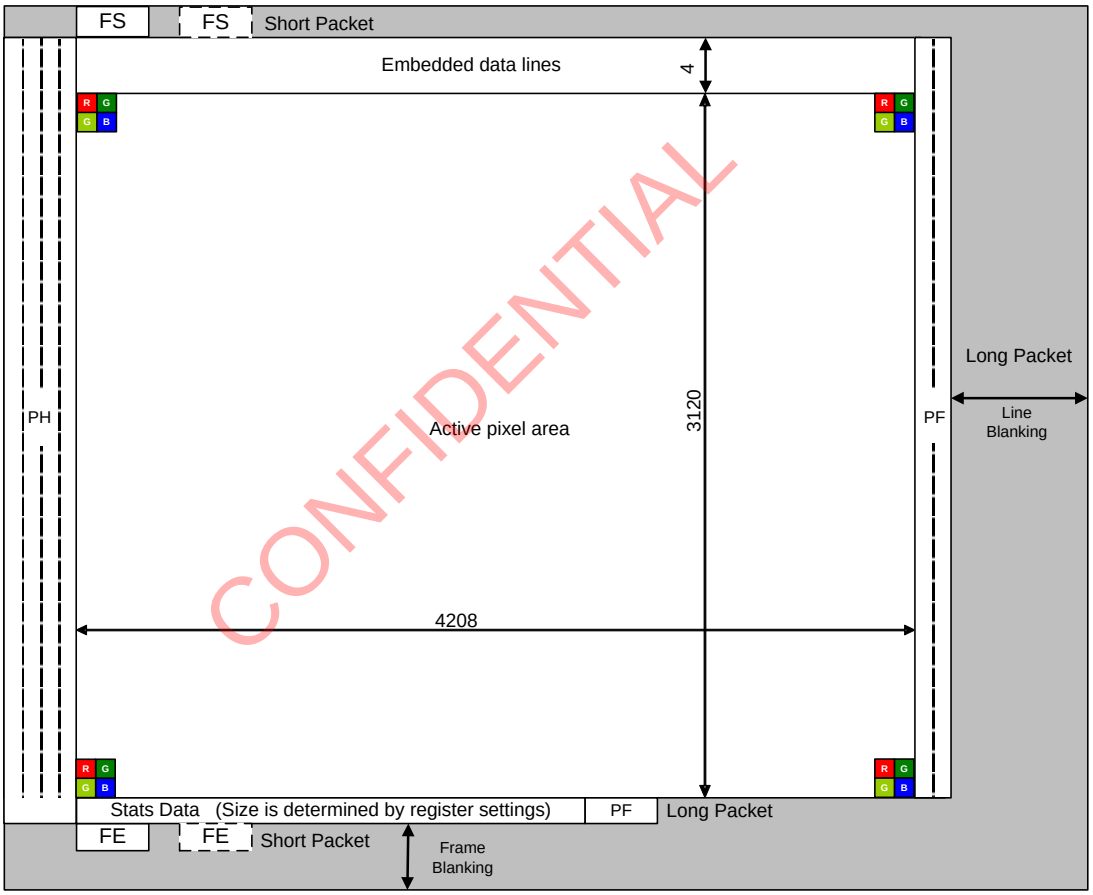


Figure 11 Color coding alignment

Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.



CONFIDENTIAL

Figure 12 Full pixel output mode data structure

If same virtual channel ID is used for both pixel and Stats data, only one FS and one FE will be generated.

Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame.
The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

STATS data control

STATS data is average value of luminance for each sub-block of a given field-of-view (FOV) setting of the sensor.
Number of sub-block is varied accrding to the size of FOV.
STATS data is 14bits values and sent via MIPI (embedded) or I2C.
The sensor can be configured to output “STATS data” during frame blanking for HDR movie use.

Image size of mode

IMX214 can capture and output full size, cropped/scaled image in combination with the normal mode or HDR mode.
Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

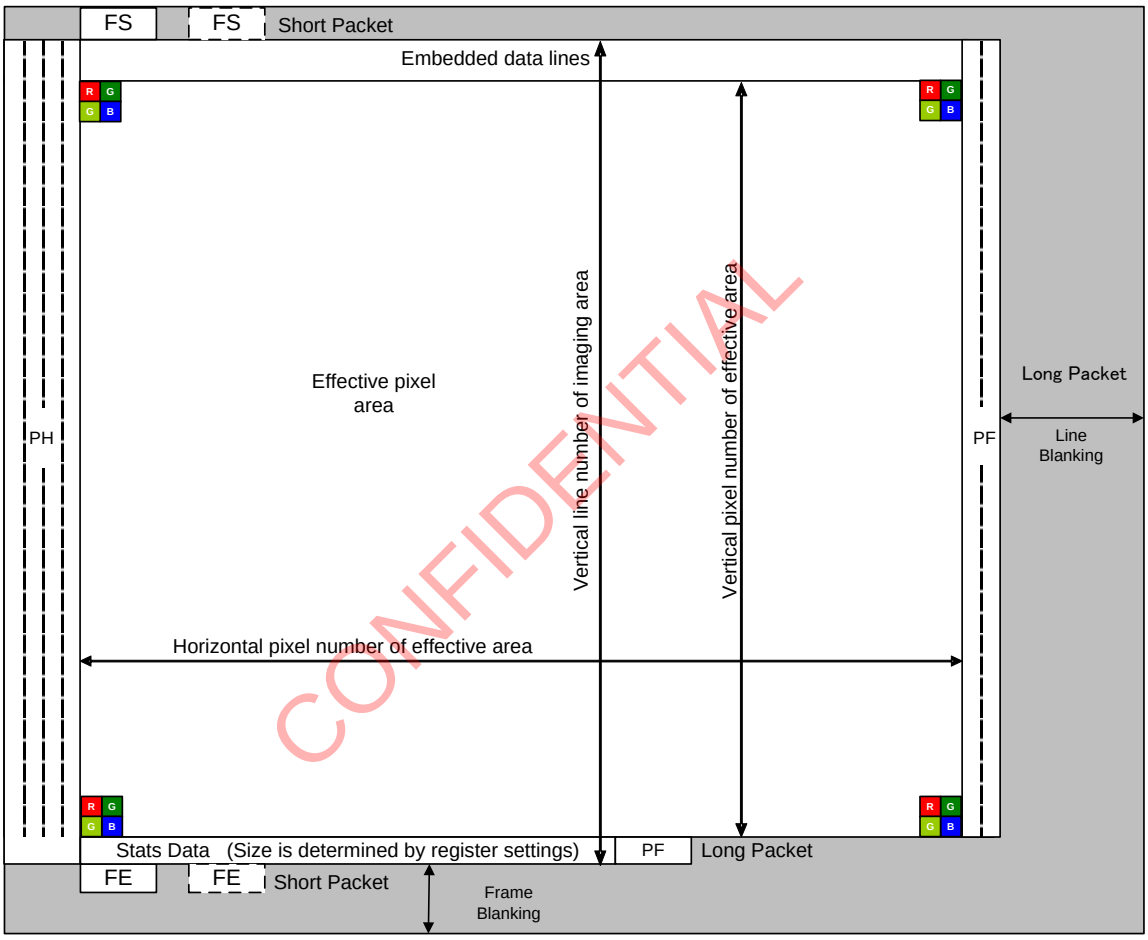


Figure 13 Image size parameter definition

Table 6 modes and image sizes

		modes									
		All-pixel		Binning (V:1/2, H:1/2)		HDR (Full-pixel)		HDR (V:1/2, H:1/2)		Binning (V:1/4, H:1/4)	
Vertical line number of imaging area		3124~3126		1564~1566		3124~3126		1564~1566		784~786	
Horizontal pixel number of effective area		4208		2104		4208		2096		1052	
Number of lines and start position		start position	Number of lines	start posiition	Number of lines	start position	Number of lines	start position	Number of lines	start positio n	Numbe r of lines
name of the areas	Frame Start	1	1	1	1	1	1	1	1	1	1
	Embedded data lines	2	4	2	4	2	4	2	4	2	4
	Vertical pixel number of effective area	6	3120	6	1560	6	3120	6	1560	6	780
	Stats Data					3126	0,1	1566	0,1	784	0,1,2
	Frame End	3126	1	1566	1	3126~31 27	1	1566~1567	1	784~7 86	1

* See Application Note or consult with support window of our sales representative about Horizontal size of HDR.

Description about operation mode

IMX214 has five modes that All-pixel, binning (V:1/2, H:1/2) , binning (V:1/4, H:1/4) and, HDR(Full pixel) and HDR (V:1/2, H:1/2).

CONFIDENTIAL

Image area control capabilities

As control fuction for image's viewing area and /or image size, IMX214 has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.

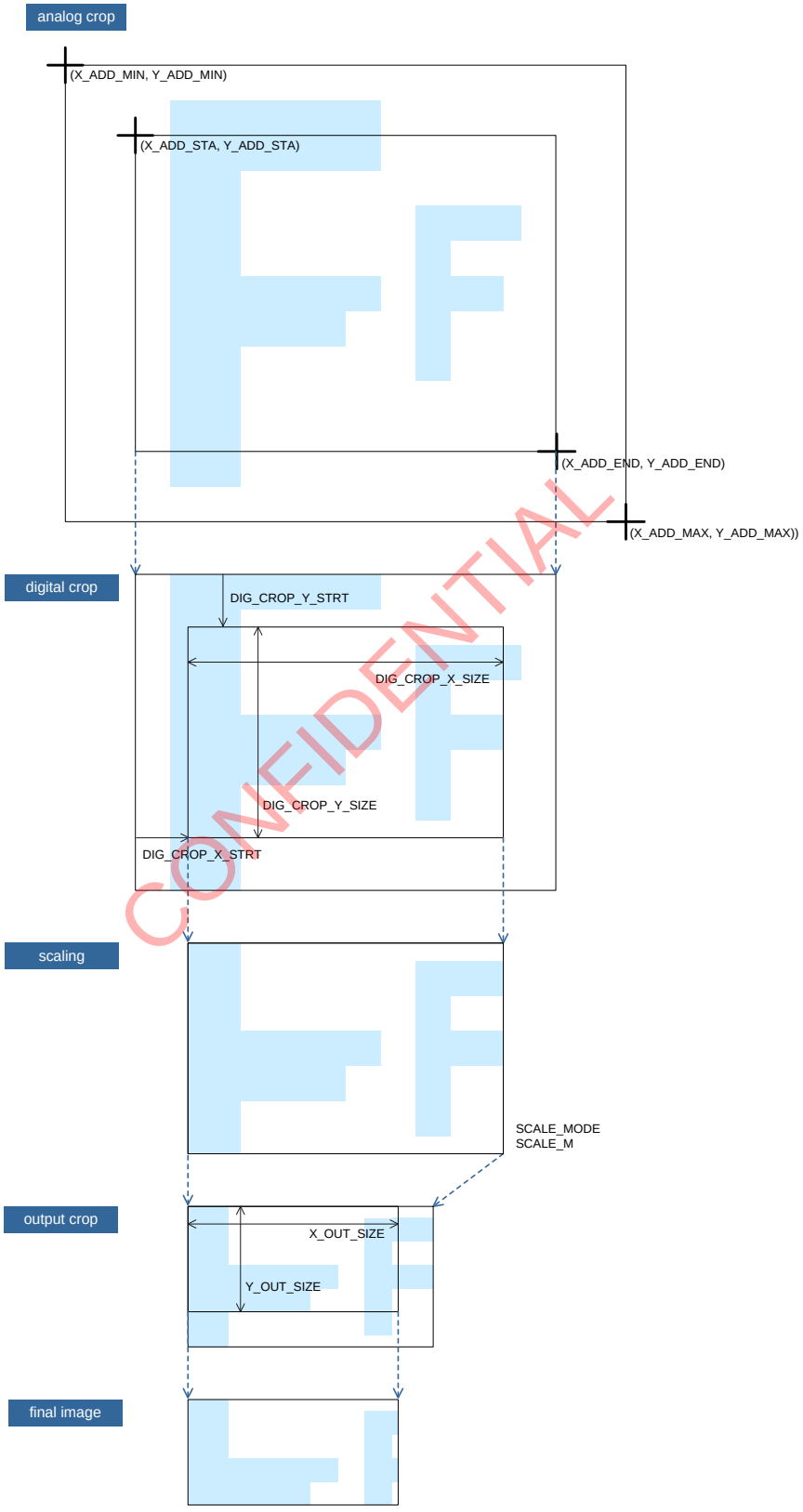


Figure 14 image area control capabilities

CONFIDENTIAL

Readout Start Position

Default readout position of IMX214 starts from the lower left when PIN1 is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper right corner.

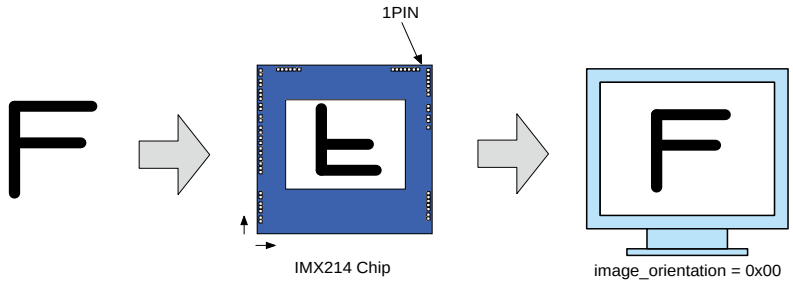
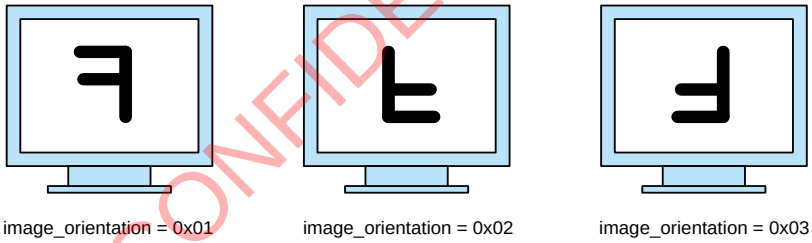


Figure 15 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changes with it.



CONFIDENTIAL

Figure 16 Read out image for each combination of flip and mirror

Gain setting

IMX214 can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 7 Range of Gains

	Max.
Analog Gain	18dB (24dB)*
Digital Gain	24dB

* When AD input is doubled for vertical analog addition-average mode, analog gain can be set up to 24dB.

Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There are two areas; one for Sony's factory area, another for module vendors.
The dynamic defect correction eliminates any critical defects detected on RGB pixel array by estimating from surrounding adjucent pixels value.

Adaptive Tone Reproduction (ATR)

Addaptice Tone Reproductio (ATR) function converts a 14 bit HDR image to a 10 bit range image using adaptive tone curve. It is active in HDR movie operation, HDR still image capture or HDR preview mode.

Chroma Noise Resuction (CNR)

Chroma Noise Reduction (CNR) mainly reduces chroma noise.

Luminance Noise Resuction (LNR)

Luminance Noise Reduction (LNR) mainly reduces optical shot noise.

CONFIDENTIAL

Miscellaneous functions

IMX214 has the following additional functions to be used for various final products' features.

See Application Notes for more details of each function.

Thermal Meter

This fumction is to measeur the themal data from internal sensor then average it. Measurement results could be read via I2C or EBD data.

Test pattern output and type of test pattern

IMX214 can output test pattern of SMIA specification by build-in pattern generator.
Test pattarns of Solid Color, 100% Color Bar, Fade to Gray Color Bar, PN4 and PN31 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

Long Exposure Setting

IMX124 can achieve a vey long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

OTP (One Time Programable Read Only Memory)

Total of 8K bit of OTP is available for users. It is devided into 16 pages and 15 pages of them are usable at user's discretion while 16th pare is asigned as the area for defective pixel correction, SMIA model ID, and partially write protected. See OTP manual for details.

3D Mode

IMX214 supports synchronized shooting opereation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method.

Flash light control sequence

IMX214 can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

External pixel power supply capability

IMX214 can select internal connection or external power supply for pixels. Sony's recommendation is "external" becase of smaller form factor due to less capacitor. Corresponding supply pins are VPI1 and VPI2.
The selection of internal or external shall be made by register setting. See IMX214 Module Design Reference Manual for more detail.

Image signal interface

MIPI transmitter

IMX214 outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.01.00 and MIPI Alliance Specification for D-PHY version 1.00.00 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

CONFIDENTIAL

How to operate IMX214

Power on Reset

IMX214 has the built in “Power On Reset” function.
It automatically initializes the internal circuit by itself when XCLR pin is open and the power supplies are brought up.
In addition, if XCLR pin is set to low and the power supplies are bring up. The sensor will skip executing the “Power On Reset” function.

Power on sequense

Power on slew rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during ower on.

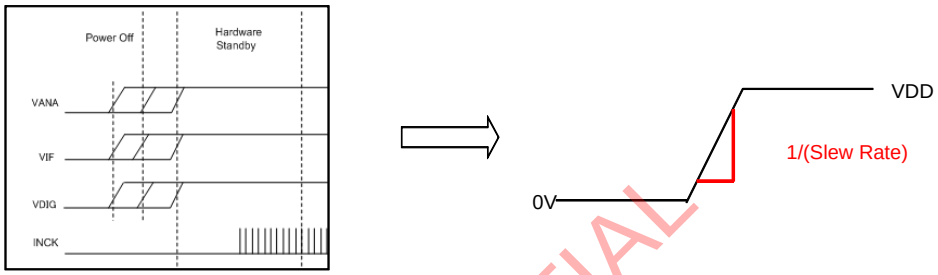


Figure 17 Power on slew rate

CONFIDENTIAL

Table 8 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF VDIG		100	mV/us	

Start up sequence with 2-wire serial communication

Please follow the power supply start up sequence below.

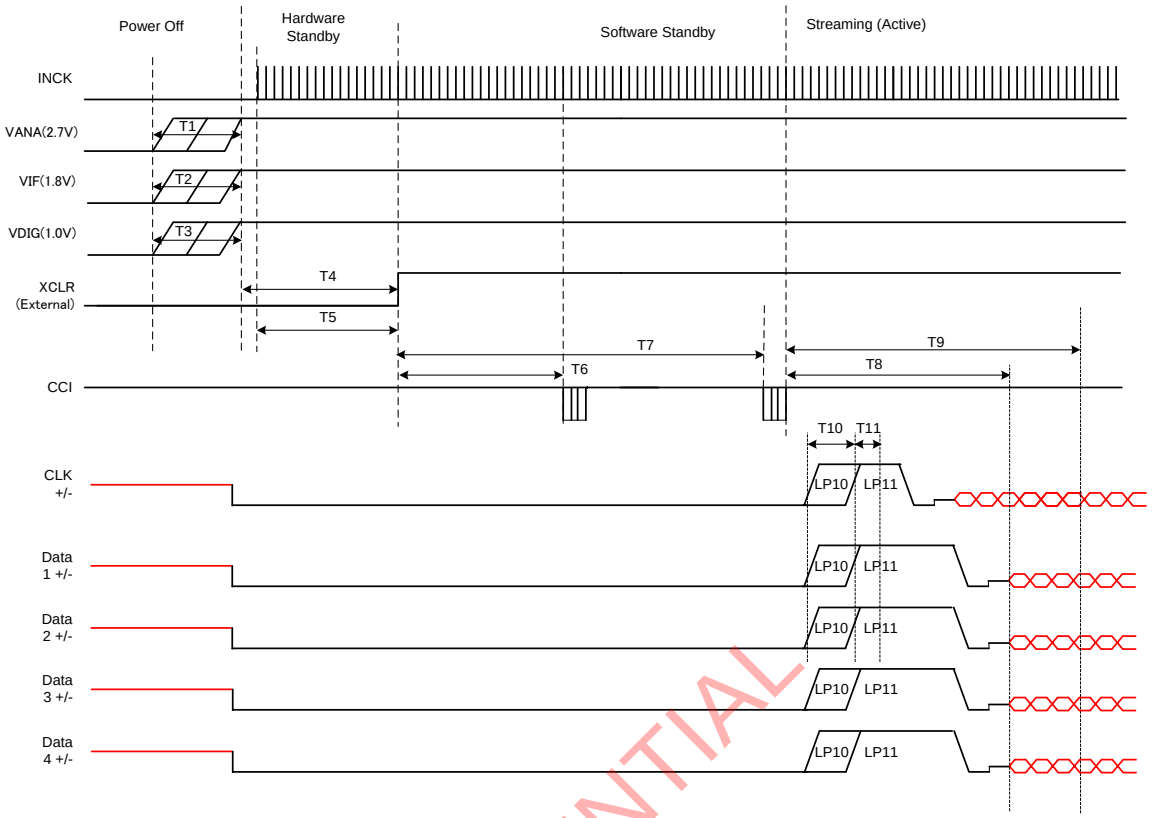


Figure 18 Start up sequence with 2-wire serial communication (external reset)

* Presence of INCK during Power Off is acceptable despite of above chart.

CONFIDENTIAL

Table 9 Start up sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA on	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rata of VANA, VDIG and VIF (0%-100%) : max100mv/us
VDIG rising – VDIG on	T2			µs	
VIF rising – VIF on	T3			µs	
VANA and VDIG and VIF rising– XCLR rising	T4	0		µs	Later of T1, T2, T3
INCK start – XCLR rising	T5	0		Ms	
XCLR rising till CCI Read Version ID register wait time	T6	1		ms	
XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	10.3		ms	
	T8		3.8 ms + The delay of the coarse integration time value +32H		
Entering Streaming Mode – First Frame Start Sequence of good quality frame in first powerup including initialization delays. All frames outputted shall have good quality.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1,1	ms	
DPHY init	T11	100	110	us	

Note) ◆ XSHUTDOWN needs to be Low until all power supplies complete power-on

CONFIDENTIAL

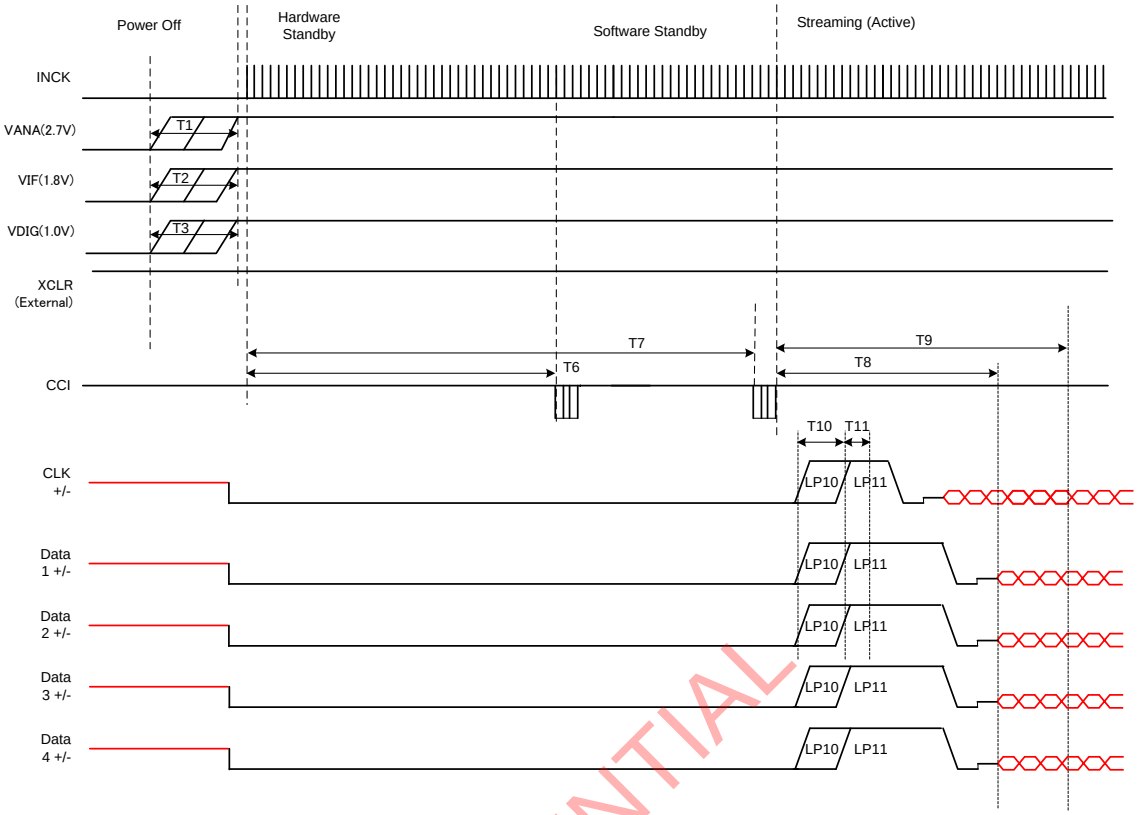


Figure 19 Start up sequence with 2-wire serial communication (power on reset)

* Power on slew rate of any power line shall not be slower than 7mV/usec if INCK is present during Power Off.

CONFIDENTIAL

Table 10 Start up sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA on	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rata of VANA, VDIG and VIF (0%-100%) : max100mv/us
VDIG rising – VDIG on	T2			µs	
VIF rising – VIF on	T3			µs	
VANA and VDIG and VIF rising and INCK start till CCI Read Version ID register wait time	T6	1		ms	
XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	10.3		ms	
	T8		3.8 ms + The delay of the coarse integration time value +32H		
Entering Streaming Mode – First Frame Start Sequence of good quality frame in first powerup including initialization delays. All frames outputted shall have good quality.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1,1	ms	
DPHY init	T11	100	110	us	

Constrains of XCLR

XCLR must remain low when VIF (IOVDD) is off.

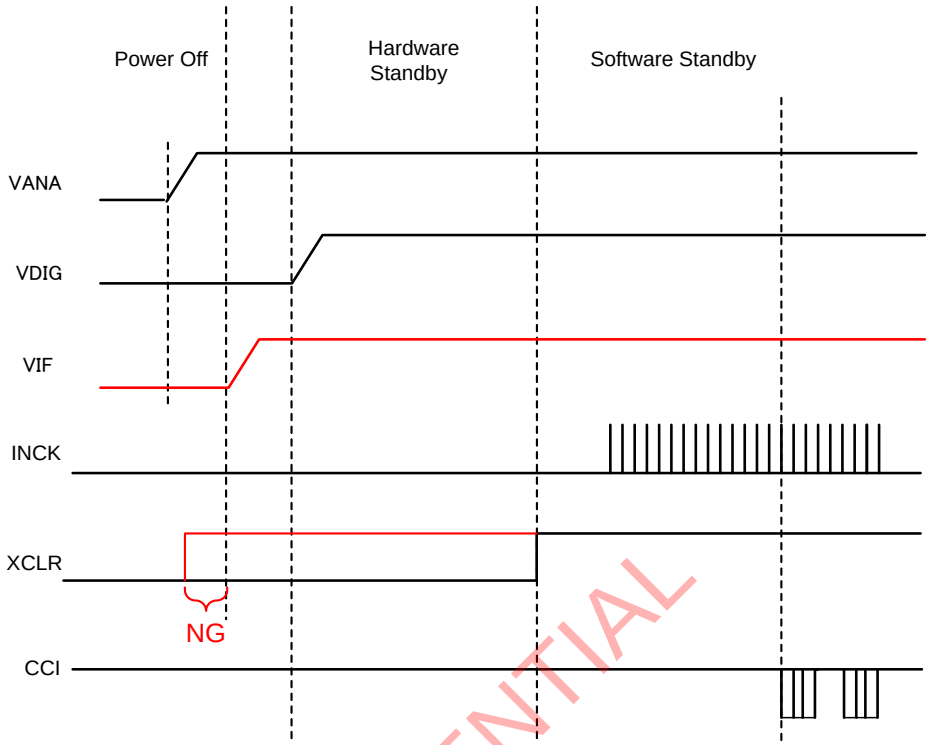


Figure 20 Constrains of XCLR in Start up sequence

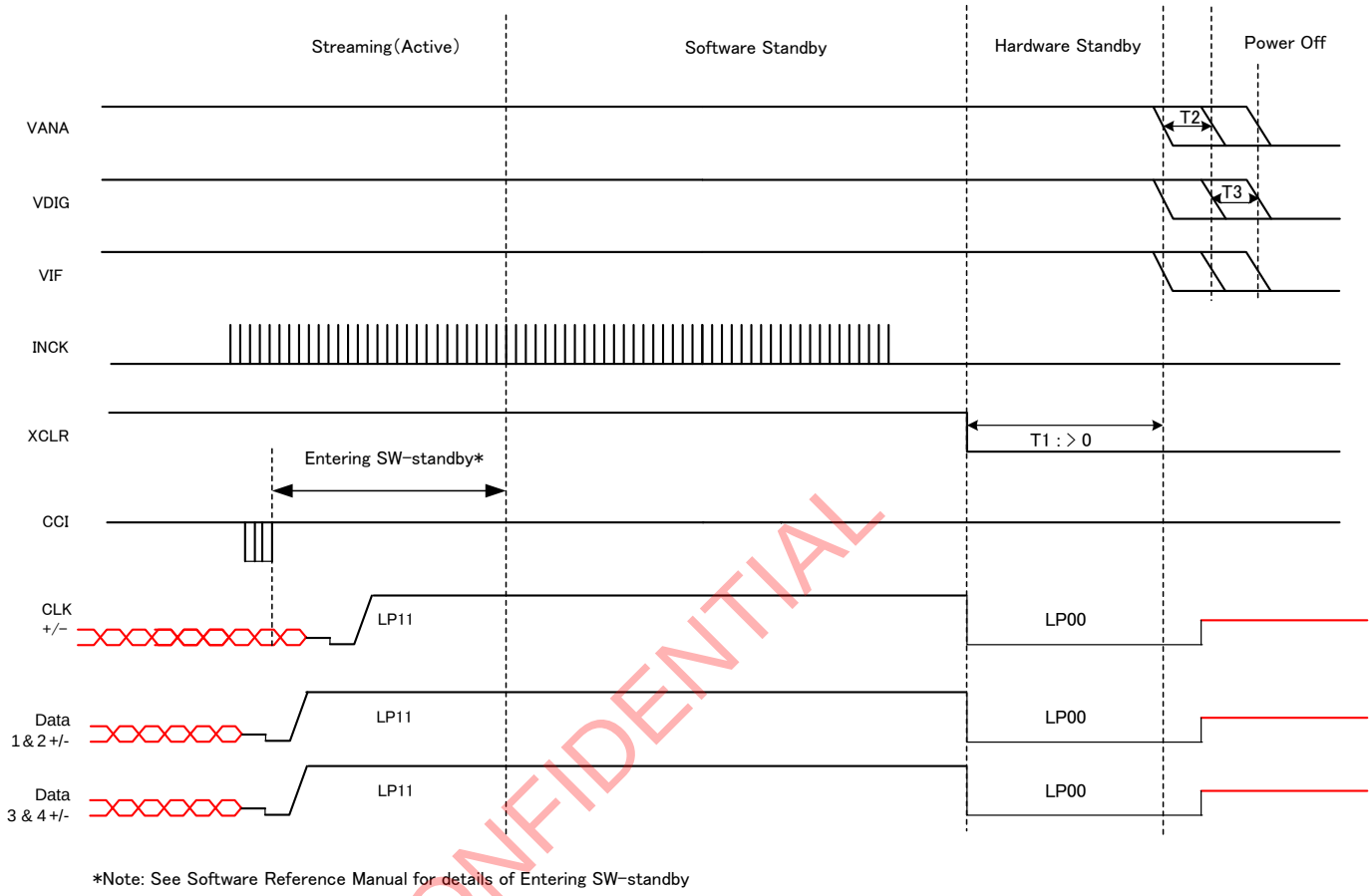
※Iignore this constraint if XCLR is not controlled externally (XCLR is open).

CONFIDENTIAL

Power down sequence

Power down sequence with 2-wire serial communication

Follow the power down sequence below.

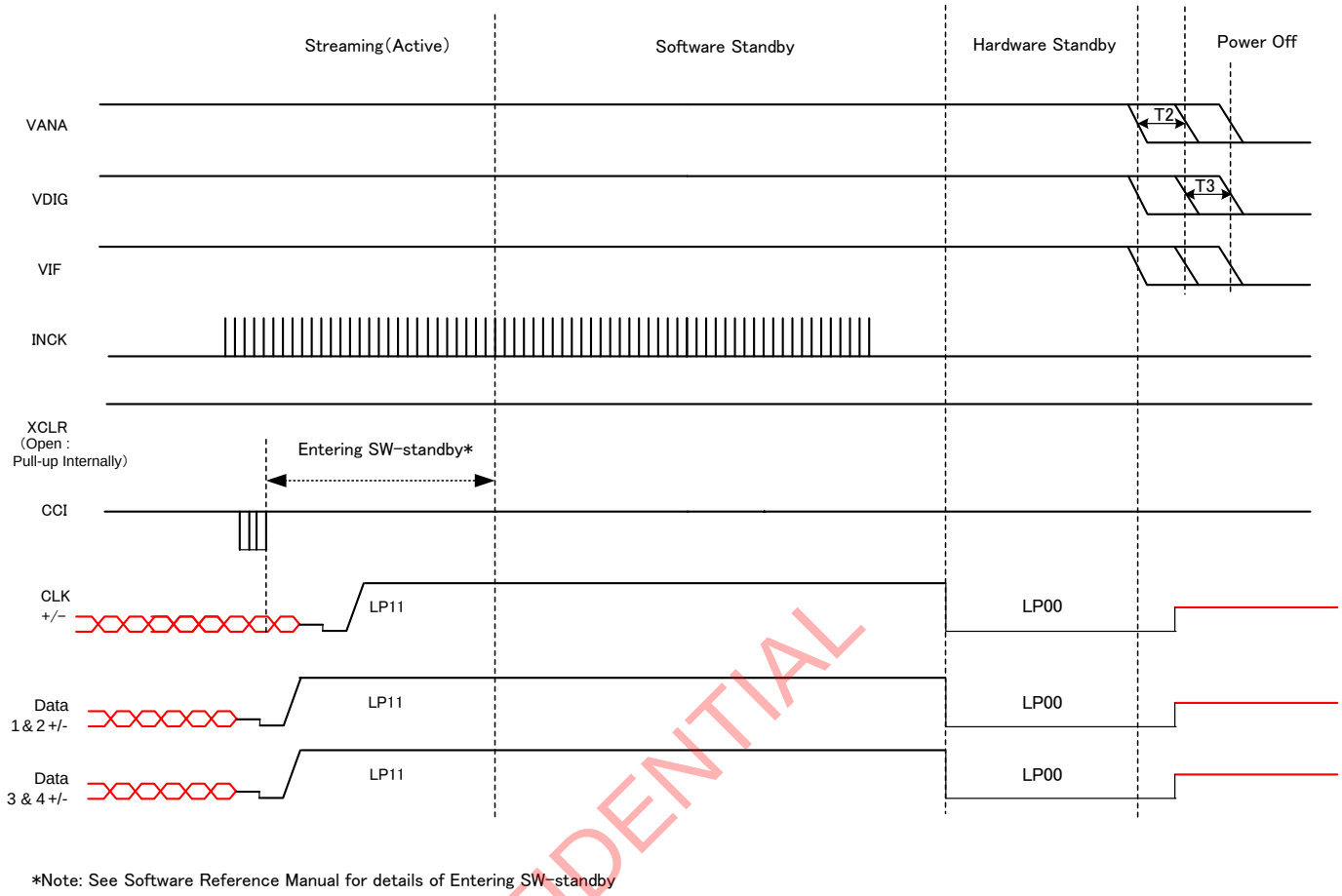


CONFIDENTIAL

Figure 21 Power down sequence with 2-wire serial communication (external reset)

Table 11 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
Internal POR negedge - VANA (VDIG or VIF) fall	T1	0		ns	
Sequence free of VANA falling and VDIG falling and VIF falling	T2, T3	VANA and VDIG and VIF may fall in any order.		ns	



CONFIDENTIAL

Figure 22 Power down sequence with 2-wire serial communication (power on reset)

Table 12 Power down sequence timing constraints (2-wire serial communication mode with power on reset)

Item	Label	Min.	Max.	Unit	Comment
Sequence free of VANA falling and VDIG falling and VIF falling	T2, T3	VANA and VDIG and VIF may fall in any order.		ns	

Constrains of XCLR

XCLR must remain low when VIF (IOVDD) is low.

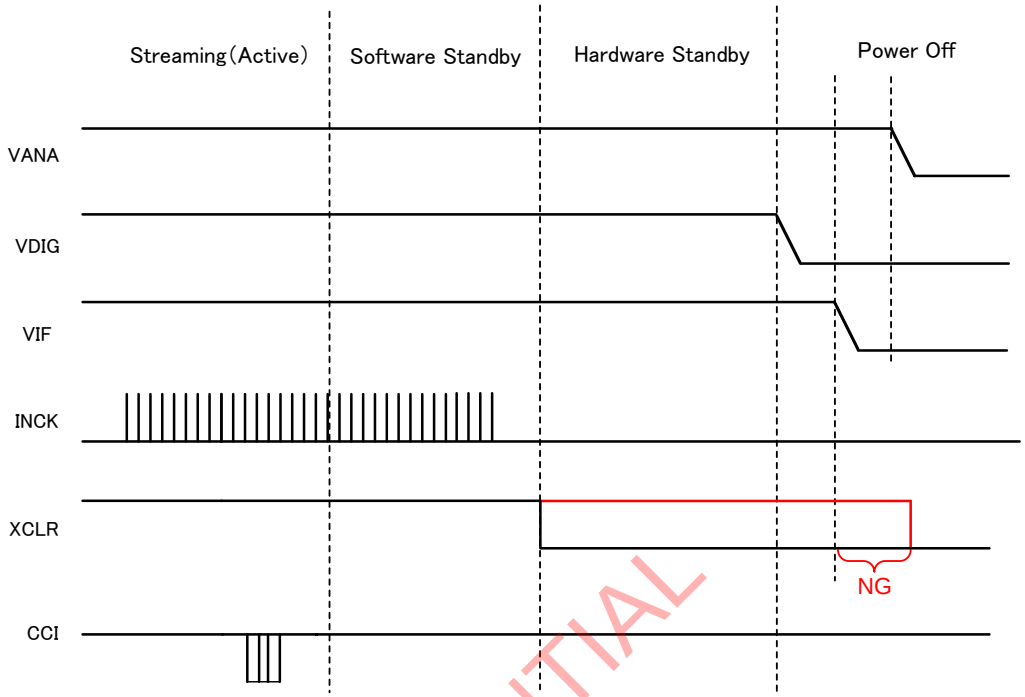


Figure 23　Constrains of XCKR in Power down sequence

※Iignore this constraint if XCLR is not controlled externally (XCLR is open).

CONFIDENTIAL

Register Map

See Register Map.

Electrical Characteristics

The Electrical Characteristics of the IMX214 is shown below

DC characteristics

Table 13 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUBD VDDHCM1,2 VDDHSN1,2,3 VDDHAN VDDHCP VPI1,2 *1)	VANA		2.6	2.7	2.9	V
	VDDLCN1,2 VDDLSC1,2,3,4,5,6,7, VDDLIO1,2	VDIG		0.9	1	1.15	V
	VDDMIO1,2,3,4,VDD	VIF		1.7	1.8	1.9	V
Digital input voltage	SDA SCL	VIH		0.7VIF		2.9	V
		VIL		-0.3		0.3VIF	V
Digital input voltage	XCLR INCK (EXTCLK)	VIH		0.65VIF		VIF + 0.3	V
		VIL		-0.3		0.35VIF	V
Digital output voltage	SDA SDO	VOH		VIF-0.4			V
		VOL				0.4	V

Note: 1) Applies only in case VPI1, 2 are externally applied (register setting is required)

CONFIDENTIAL

AC Characteristics

Master Clock Waveform Diagram

INCK (EXTCLK) Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK (EXTCLK).

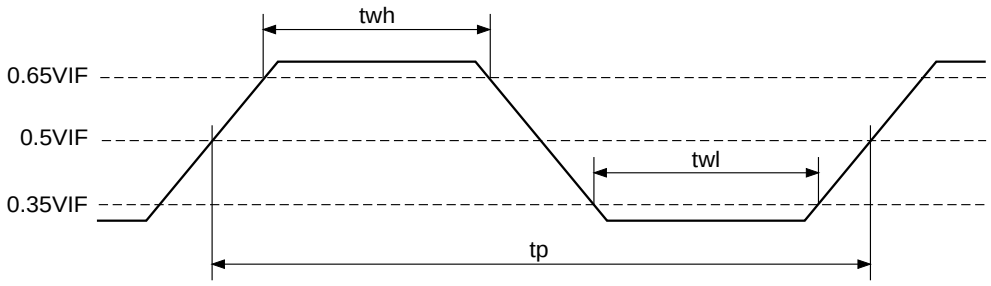


Figure 24 Master Clock Square Waveform Input Diagram

Table 14 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK (EXTCLK) clock frequency	f_{SCK}	6		27	MHz
INCK (EXTCLK) clock period	t_p	37		166.7	ns
INCK (EXTCLK) low level width	t_{wl}	0.4tp		0.6tp	ns
INCK (EXTCLK) high level width	t_{wh}	0.4tp		0.6tp	ns
INCK (EXTCLK) jitter	Tjitter			600	ps

INCK (EXTCLK) Sine Waveform Input Specifications

IMX214 does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 15 PLL block characteristics (VTsystem)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		27.0	MHz	
VCO frequency range	338.0		1200.0	MHz	
Output frequency range	338.0		1200.0	MHz	
Settling time			200.0	µs	

CONFIDENTIAL

Table 16 PLL block characteristics (OPsystem)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	1.0		27.0	MHz	
VCO frequency range	338.0		1200.0	MHz	
Output frequency range	338.0		1200.0	MHz	
Settling time			900.0	µs	

Conditions) V_{ANA} = 2.7 V, V_{DIG} = 1.0 V, Tj = 25 ˚C, Output frequency = 1200 MHz.

Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

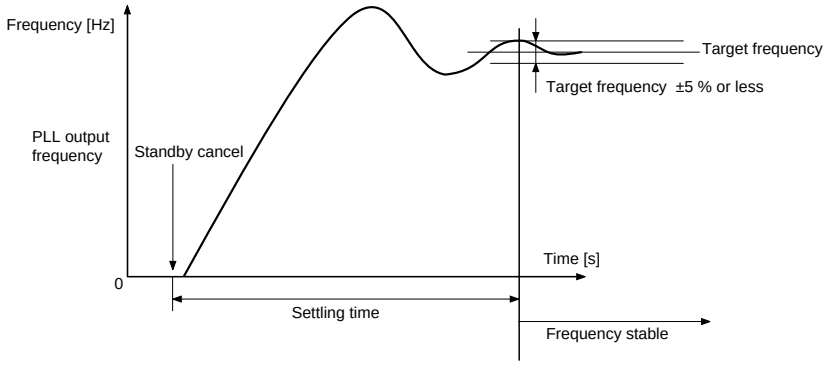


Figure 25 Definition of settling time

2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

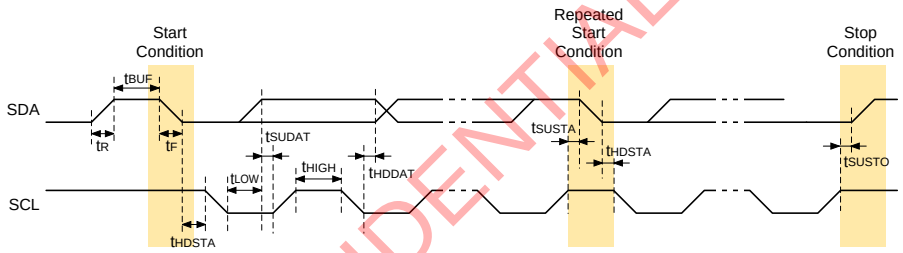


Figure 26 2-wire serial communication block specification

CONFIDENTIAL

Table 17 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low level input voltage	V_{IL}		-0.3	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V,Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V,Sink 3 mA	0	$0.2V_{IF}$	V
High level output voltage	V_{OH}		V_{IF} - 0.4		V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	μA
SDA I/O capacitance	$C_{I/O}$			8	pF
SCL Input capacitance	C_I			6	pF

Table 18 2-wire serial communication block AC specification

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	—	300	ns
Fall time (SDA and SCL)	t_F	—	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	—	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	—	µs
Setup time (stop condition)	t_{SUSTO}	0.6	—	µs
Data setup time	t_{SUDAT}	100	—	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Current consumption and standby current

Table 19 Current consumption and standby current

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.0 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		39.2	44.7	mA	
Current consumption (digital)	I_{DIG}		76.7	140.3	mA	DPC, HDR, LNR, CNR function off
Standby current (analog)	I_{STBANA}			43.1	µA	XCLR (XSHUTDOWN) : Low fixed INCK (EXTCLK) :stop
Standby current (digital)	I_{STBDIG}			58.2	mA	XCLR (XSHUTDOWN) : Low fixed INCK (EXTCLK) :stop
Standby current (IF)	I_{STBIF}			48.7	µA	XCLR (XSHUTDOWN) : Low fixed INCK (EXTCLK) :stop

CONFIDENTIAL

Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

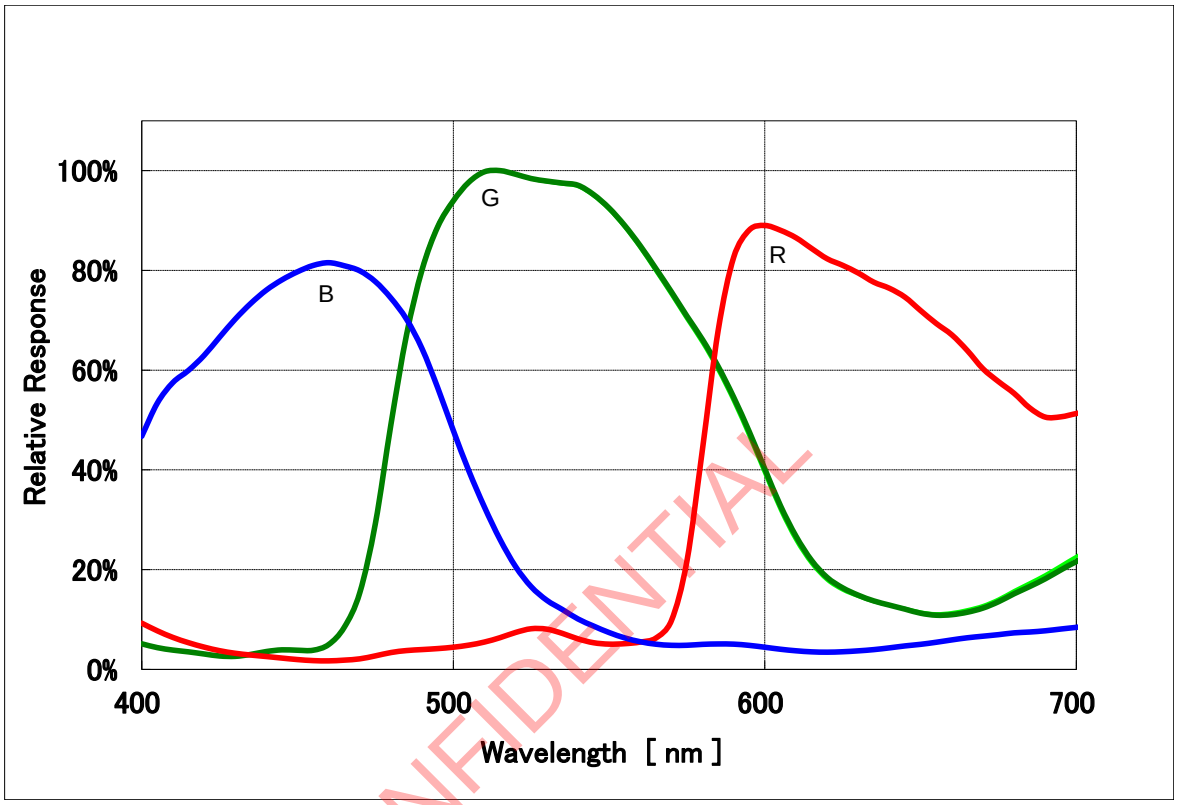


Figure 27 Spectral sensitivity characteristics

CONFIDENTIAL

Image Sensor Characteristics

Image Sensor Characteristics

Table 20 Image Sensor Characteristics

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.0 V, V_{IF} = 1.8 V,Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	170			LSB	Center	1(*)	1/120 s storage
Sensitivity ratio	RG	0.49	0.55	0.61		Center	2(*)	
	BG	0.37	0.43	0.49				
Saturation signal	Vsat	1023			LSB	Zone1	3(*)	
Video signal shading	SH			70	%	Zone2D	4(*)	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	5(*)	When operation at 15 frame/s

(*)These refer to the descriptions of the Measurement Methods on Page 43.

LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value). The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Zone Definition used for specifying image sensor characteristics

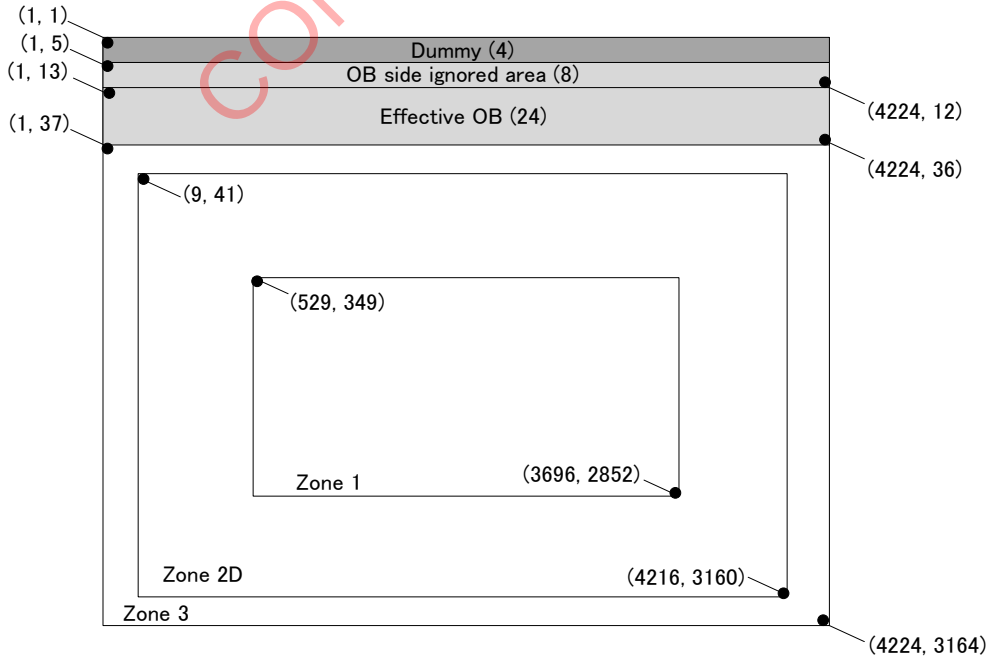


Figure 28 Zone Definition Diagram

CONFIDENTIAL

Measurement Method for Image Sensor Characteristics

Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 21 Measurement Conditions

Supply voltage	Analog 2.7 V, digital 1.0 V, IF 1.8 V
Clock	INCK (EXTCLK) 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.
As an example of 1 LSB, the typical value is 1 LSB ≈ 0.355 mV in all-pixel output 10-bit operation mode. The minimum value is 0.327 mV and the maximum value is 0.376 mV.

Color Coding of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.
All pixel signals are output successively in a 1/15 s period.

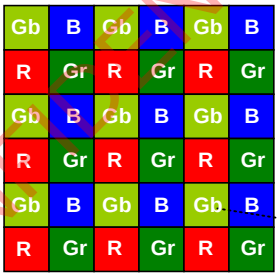


Figure 29 Color coding alignment

CONFIDENTIAL

Definition of Standard Imaging Conditions

Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

Standard imaging condition III

A recommended testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

Measurement method

Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the luminous intensity of 10 times that of the standard imaging condition and the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb) /2) × (300/120)} [LSB]

Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 300 LSB, measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 300 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 300 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax – Gmin) /Gmax) × 100 [%]

Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

CONFIDENTIAL

Spot Pixel Specification

Table 22 Spot Pixel Specifications

(15 frame/s, VANA = 2.7 V, VDIG = 1.0 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone				Measurement method	Remarks
		Zone2D	Zone3	Ineffective OB	Effective OB		
Black or white pixels at high light	30 % ≤ D	65	No evaluation criteria applied			2	
White pixels in the dark	28 (LSB) ≤ D	975	No evaluation criteria applied			2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, HDR, LNR, CNR) disabled..
4. The maximum quantity pixel counts of 65 for Bright Pixels and 975 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any colour channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “White and Black Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the White and Black Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

CONFIDENTIAL

Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.") Cosmic radiation is one of the causes of White Pixels. Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference] The Annual number of White Pixels Occurrence Caused by Cosmic Radiation
The data in the below chart shows the estimated annual number of White Pixels occurrence caused by cosmic radiation in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 ℃)	Annual number of occurrence
5.6 mV or higher	1.3 pcs
10.0 mV or higher	0.8 pcs
24.0 mV or higher	0.4 pcs
50.0 mV or higher	0.2 pcs
72.0 mV or higher	0.2 pcs

CONFIDENTIAL

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

Note 4) As this data does not take occurrence of White Pixels caused by alpha radiation into account, White Pixels are likely to occur at higher value than the rate set forth in such data.

For Your Reference:
The annual number of White Pixels occurrence caused by cosmic radiation at an altitude of 3,000 meters will be from 5 to 10 times higher than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence caused by cosmic radiation in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

Spot Pixel Pattern Specifications

Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 367 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B), and substitute the values into the following formula.
The 367LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

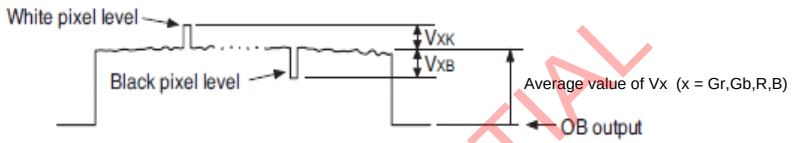


Figure 30 Measurement Method for Spot Pixels

White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

CONFIDENTIAL

CRA Characteristics of Recommended Lens

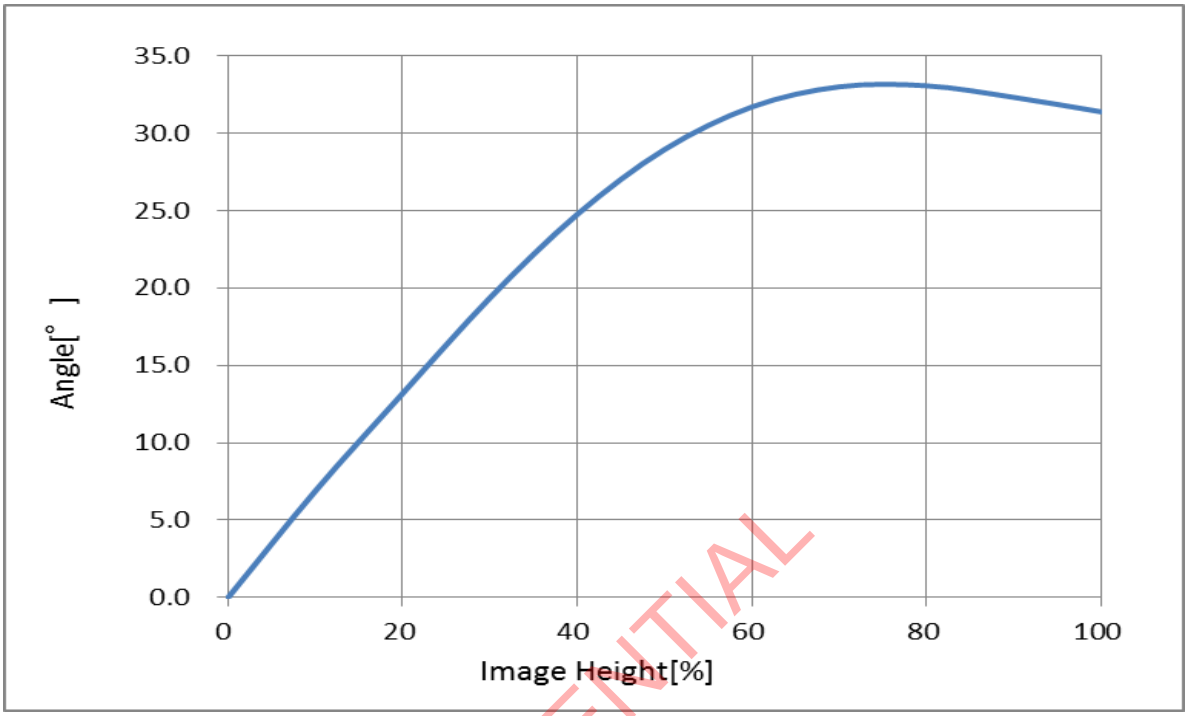


Figure 31 CRA characteristics

CONFIDENTIAL

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

CONFIDENTIAL

Notes of Caution

1. Prohibited Area for the Contact of Collet

-Edge of Chip (Dust generation)
-Unit Cell Area
-Die Pad (Electrostatic destruction)
-Around the Die Pad (Coating damage)
Note: Please ensure clearance considering the accuracy at the time of pick up.
*Clearance 150 µm or more recommended.

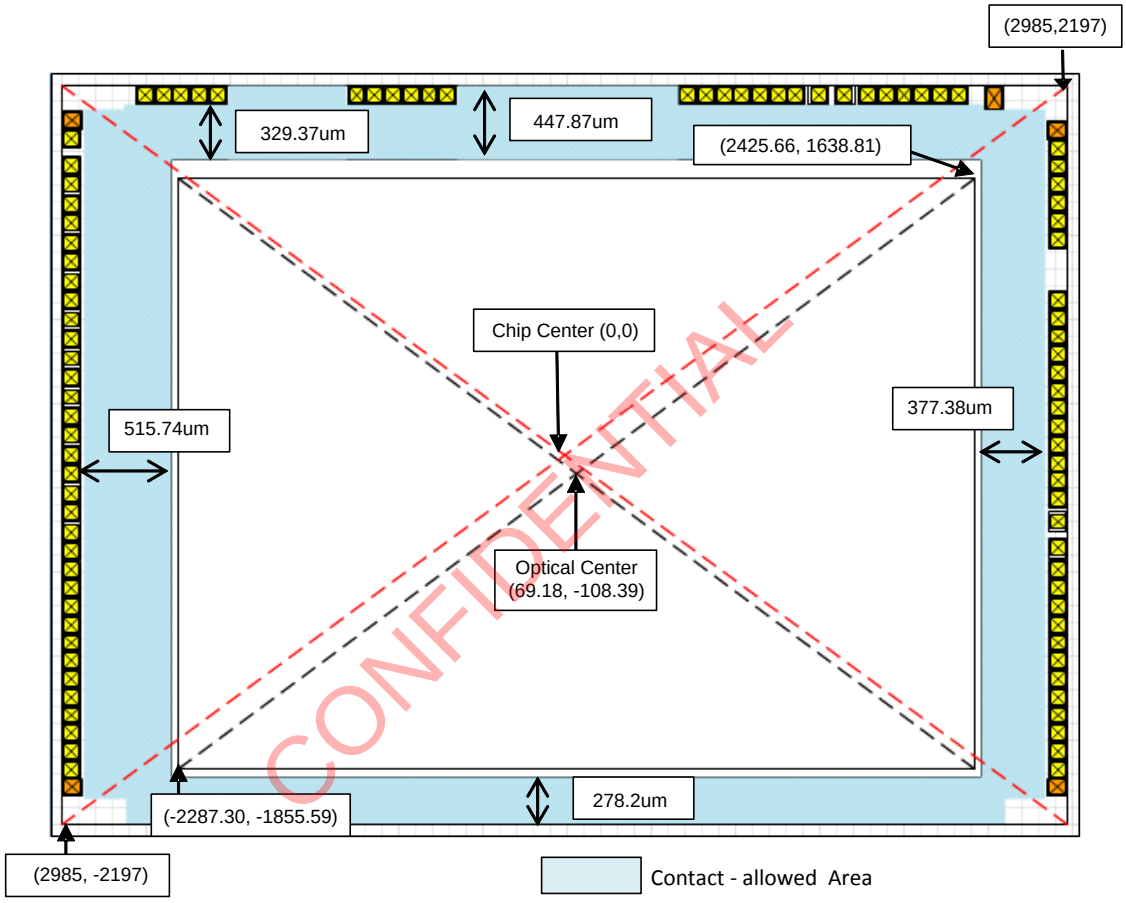


Figure 32 Prohibited Area

2. Ultrasonic cleaning is prohibited after chip-die bonded.

CONFIDENTIAL